

DEVICE PARAMETERS 1/

JPL PART #	MFR	GENERIC PART NO.	RADIATION LEVEL (TID) (RADS) 2/	PACKAGE STYLE	TERMINAL CONNECTIONS	ELECTRICAL PERFORMANCE CHARACTERISTICS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CONNECTION TABLE
12169-E01060FR	HONEYWELL SSEC	HR1060 - SSRIU	100K	FIG. 5-3 HEREIN (256-LEAD FLATPACK)	FIG. 5-1 HEREIN	TABLE 4-4 & 4-5 HEREIN	TABLE 4-1 HEREIN	TABLE 4-7 HEREIN

- NOTES: 1/ THIS DRAWING, IN CONJUNCTION WITH CS515837B AND MIL-I-38535, LEVEL V, IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES.
 2/ THE POST-IRRADIATION PARAMETRIC LIMITS SHALL BE THOSE OF TABLES 4-4 & 4-5 HEREIN.
 3/ THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)			ST 12169	REV. A
SHEET 2		SHEET 2				

TABLE OF CONTENTS

Scope.....5

Applicable Documents.....5

1. CHIP OVERVIEW.....6

2. SSRIU ASIC SIGNAL DESIGNATIONS AND DESCRIPTIONS8

3. FUNCTIONAL DESCRIPTION.....13

 3.1 Functional Overview.....13

 3.2 SSRIU Interfaces14

 3.3 SSRIU Buffers14

 3.3.1 SSR Command Buffer.....14

 3.3.2 SSR Record Buffer.....14

 3.3.3 SSR Playback Buffer.....14

 3.3.4 SSR Status Buffer.....14

 3.3.5 Downlink Buffers A and B.....14

 3.4 SSRIU Timing15

 3.4.1 Command Interface Timing.....15

 3.4.2 Record Interface Timing15

 3.4.3 Playback Interface Timing16

 3.4.4 Status Interface Timing16

4. ELECTRICAL CHARACTERISTICS17

 4.1 Electrical Test Requirements17

 4.2 Absolute Maximum Ratings.....18

 4.3 Recommended Operating Conditions18

 4.4 DC Characteristics19

 4.4.1 DC Electrical Performance Characteristics19

 4.4.2 Estimated Power Dissipation.....20

 4.4.3 IDDQ Testing.....20

 4.4.4 Pulldown Resistors.....20

 4.4.5 Pullup Resistors.....21

 4.4.6 Open Drain Outputs.....21

 4.5 AC Characteristics22

 4.5.1 AC Electrical Performance Characteristics22

 4.5.2 Timing Analysis.....22

 4.5.2.1 Pre-Layout Timing Margins.....22

 4.5.2.2 Post-Layout Timing Margins.....23

 4.5.2.3 Tester Specification Limits.....23

 4.5.3 Tester Load Circuit24

 4.6 Burn-In.....25

 4.6.1 Static Burn-In.....25

 4.6.2 Dynamic Burn-In.....25

 4.6.3 Burn-In Conditions.....25

 4.6.4 Burn-In Configuration.....26

 4.6.5 Delta Limits.....30

 4.7 Pin Type Description30

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 3			SHEET 3

5. PHYSICAL CHARACTERISTICS	31
5.1 Pin Assignment.....	31
5.2 Bonding Diagram	32
5.3 Package Outline.....	33
5.4 Marking Diagram	34

LIST OF TABLES

Table 2-1. Signal Descriptions.....	9
Table 4-1. Electrical Test Requirements	17
Table 4-2. Absolute Maximum Ratings.....	18
Table 4-3. Recommended Operating Conditions	18
Table 4-4. DC Performance Characteristics.....	19
Table 4-5. AC Performance Characteristics.....	22
Table 4-6. Burn-In Conditions.....	25
Table 4-7. Burn-In Configuration	26
Table 4-8. Delta Limits	30
Table 4-9. Pin Type Description	30

LIST OF FIGURES

Figure 1-1. External Interface of the SSRIU Chip.....	6
Figure 1-2. CDEA - SSR Cross - Strap	7
Figure 2-1. SSRIU ASIC Symbol.....	8
Figure 3-1. SSRIU Block Diagram	13
Figure 3-2. SSRIU Command Interface Timing Diagram.....	15
Figure 3-3. SSRIU Record Interface Timing Diagram	15
Figure 3-4. SSRIU Playback Interface Timing Diagram.....	16
Figure 3-1. SSRIU Status Interface Timing Diagram	16
Figure 4-1. Tester Load Circuit.....	24
Figure 5-1. SSRIU ASIC Pinout Assignments	31
Figure 5-2. Bonding Diagram (256 pin Flatpack)	32
Figure 5-3. Package Outline (256 pin Flatpack).....	33
Figure 5-4. Marking Diagram.....	34

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 4			SHEET 4

Scope

This is the detailed specification for a space-qualified *Solid State Recorder Interface Unit* (SSRIU) gate array for the Command Data Subsystem. This document shall be the sole source of design specifications for the SSRIU gate array, and shall supersede any other specification documents issued prior to this release.

Applicable Documents

- o *General Specification for Gate Array Application Specific Integrated Circuits (ASICs), 24 March 1992, CS515837, Rev. B*

This document establishes the general design system, manufacturing and testing requirements for the gate array Application Specific Integrated Circuit (ASIC) parts.

- o *Solid State Recorder Interface Unit , Functional Specification, Version 2.0, February 9, 1993.*

This document is the primary source of the functional specifications of the space qualified Solid State Recorder Interface Unit (SSRIU) ASIC device for the CASSINI Mission.

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 5			SHEET 5

1. CHIP OVERVIEW

The SSRIU chip is an interface chip between the ISB, the SSR/DL Memory Buffer, and the SSR as shown in Figure 1.1. It serves as an arbiter for access to the SSR/DL memory buffer. The maximum combined output rate to the DL and to the SSR is 249Kbps which is much smaller than the ISB bandwidth of 16Mbps. Therefore, all RT transfer frames from the EFC need to be stored in the SSR/DL memory buffer before being sent to the RSDL unit. All data and commands going to the SSR reside in this memory before being sent to the SSR. Playback data and TLM status from the SSR also go to this memory before being sent to the EFC or to the RSDL unit.

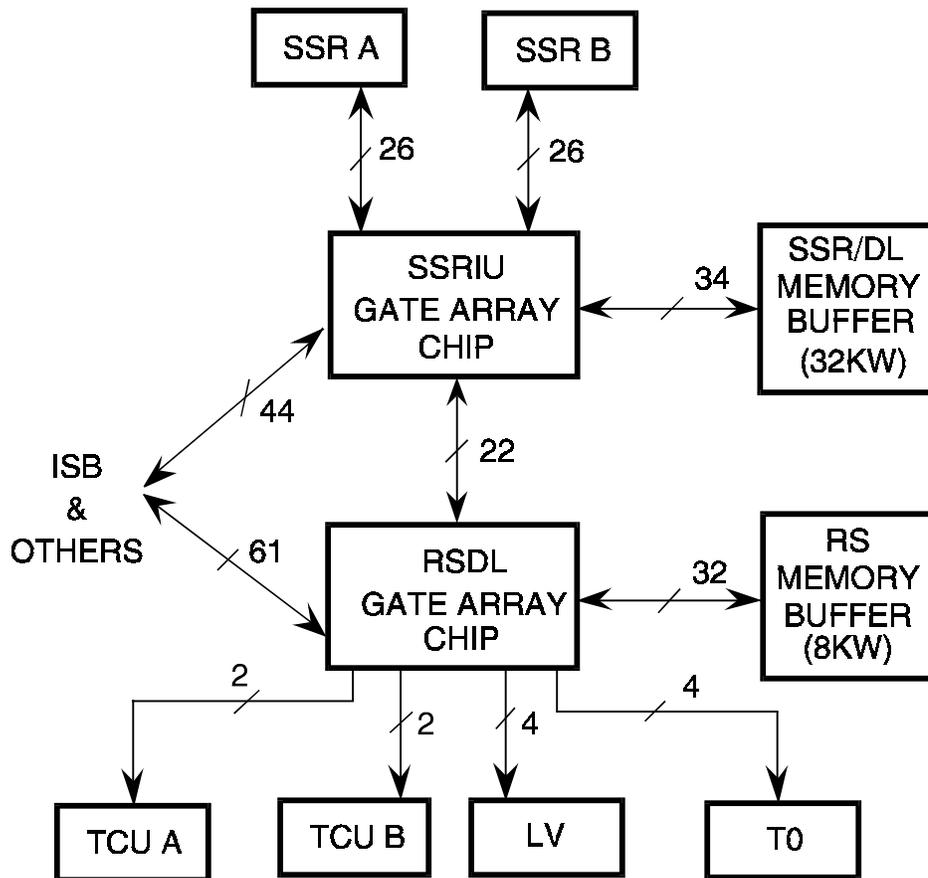


Figure 1-1. External Interface of the SSRIU Chip

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 6		SHEET 6	

The Solid State Recorder Interface Unit (SSRIU) hardware provides CDS flight software (FSW) with its only interface to the Solid State Recorder (SSR). It also provides FSW with a data interface to the Reed-Solomon Downlink (RSDL) hardware and the Downlink. The CDEA is cross-strapped to the two SSRs as shown in Figure 1-2. Note that in CDEA A, Port 1 is connected to SSR A, while in CDEA B, port 1 is connected to SSR B.

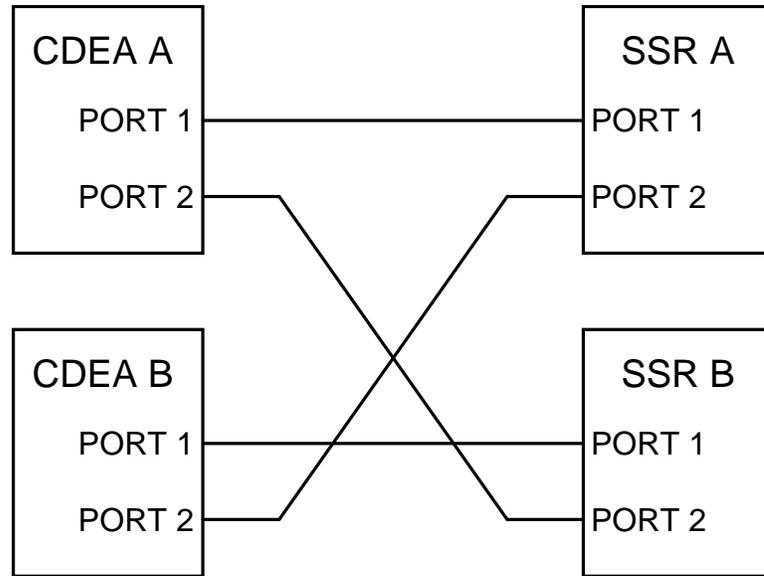


Figure 1-2. CDEA - SSR Cross - Strap

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169	REV. A
SHEET 7			SHEET 7	

2. SSRIU ASIC SIGNAL DESIGNATIONS AND DESCRIPTIONS

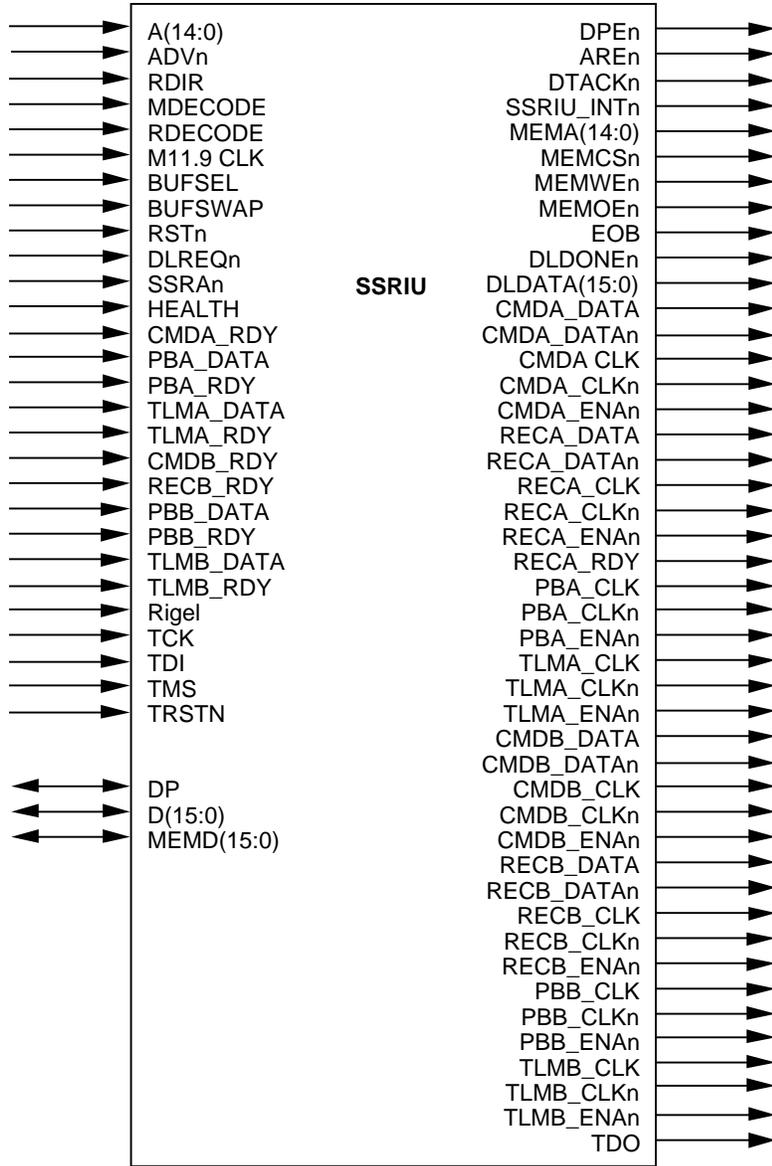


Figure 2-1. SSRIU ASIC Symbol

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 8			SHEET 8

Table 2-1. Signal Descriptions

Name	Pin No. ¹	Type ²	Description
A(14:0)	173, 174, 177, 181, 187, 198, 201, 204, 210, 216, 222, 225, 226, 229, 234	IN	ISB Address Bus (32KW).
DP	231	BI6	ISB Data Parity.
D(15:0)	176, 180, 183, 186, 189, 197, 200, 203, 206, 209, 212, 215, 218, 221, 224, 228	BI6	ISB Data Bus.
DPE _n	233	OUT6	ISB Data Parity Error. It indicates that an illegal ISB data parity has been detected during the current ISB write cycle. (open collector type of output)
ARE _n	248	OUT6	ISB Address Range Error. It indicates that the ISB is accessing an undefined register.
ADV _n	236	IN	ISB Address Valid.
RDIR	235	IN	ISB Read Direction. It indicates an ISB read cycle when it is high, an ISB write cycle when it is low.
DTACK _n	243	OUT6	ISB Data Transfer Acknowledge. It indicates that the data transfer is complete. (open collector type of output)
SSRIU_INT _n	6	OUT6	SSRIU interrupt line. It is asserted when an internal error has been detected, or any SSR transfer has been completed. The cause of the interrupt can be seen in the Interrupt Register.
MDECODE	241	IN	Select Local Memory. ISB accesses SSR/DL memory buffer. This decoded line comes from the HCD/CRC device.
RDECODE	242	IN	Select Local Register. ISB accesses SSRIU internal register. This decoded line comes from the HCD/CRC device.
M11.9_CLK	238	INPD	11.9448MHZ clock comes from the crystal.
MEMA(14:0)	94, 95, 98, 101, 107, 110, 113, 118-120, 123, 134, 137, 138, 141	OUT6	SSR/DL Memory Buffer Address Bus.
MEMD(15:0)	90, 93, 97, 100, 103, 106, 109, 112, 115, 117, 122, 125, 133, 136, 140, 144	BI6	SSR/DL Memory Buffer Data Bus.

¹ The pin numbers of bus signals are in the same sequence as the signals.

² For a description of the signal type refer to Table 4-9.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 9			SHEET 9

Table 2-1. Signal Descriptions (Cont'd)

Name	Pin No. ³	Type ⁴	Description
MEMCS _n	86	OUT6	SSR/DL Memory Buffer Chip Select.
MEMWEn	88	OUT6	SSR/DL Memory Buffer Write Enable.
MEMOEn	87	OUT6	SSR/DL Memory Buffer Output Enable.
BUFSEL	152	IN	Buffer Select for the DL buffer. 0 selects the A buffer, 1 selects the B buffer. This signal comes from the RSDL device.
BUFSWAP	76	IN	Swap the DL buffer. This signal comes from the RSDL device.
EOB	169	OUT6	End of the DL buffer. This signal goes to the RSDL device. It indicates that the end of the DL buffer has been reached.
RST _n	240	IN	Synchronous Reset. Reset the entire SSRIU device. This is the combined Hardware/Software reset. This signal comes from the RSDL device.
DLREQ _n	171	IN	DL request for memory read. This signal comes from the RSDL device.
DLDONEn	168	OUT6	DL request has been served. This signal goes to the RSDL device.
DLDATA(15:0)	145-147, 150, 151, 153, 154, 158-165, 170	OUT6	DL Data bus. This bus goes to the RSDL device.
SSRAn	52	IN	Select SSR A or B Port. 0 selects SSR A Port, 1 selects SSR B Port. This signal comes from the CRC.
HEALTH	67	IN	CDS Health. This signal prevents unhealthy CDS to access the SSR. 1 indicates that the CDS is healthy.
CMDA_DATA	74	TRIOD6	SSR Serial CMD of A Port.
CMDA_DATA _n	75	TRIOD6	SSR Serial CMD of A Port in reverse polarity.
CMDA_CLK	80	TRIOD6	SSR Clock for Serial CMD of A Port.
CMDA_CLK _n	77	TRIOD6	SSR Clock for Serial CMD of A Port in reverse polarity.
CMDA_ENAn	84	TRIOD6	SSR Enable for Serial CMD of A Port.
CMDA_RDY	83	IN	SSR Ready for Serial CMD of A Port.
RECA_DATA	73	TRIOD6	SSR Serial REC of A Port.
RECA_DATA _n	72	TRIOD6	SSR Serial REC of A Port in reverse polarity.
RECA_CLK	68	TRIOD6	SSR Clock for Serial REC of A Port.

³ The pin numbers of bus signals are in the same sequence as the signals.

⁴ For a description of the signal type refer to Table 4-9.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 10		SHEET 10	

Table 2-1. Signal Descriptions (Cont'd)

Name	Pin No. ⁵	Type ⁶	Description
RECA_CLKn	62	TRIOD6	SSR Clock for Serial REC of A Port in reverse polarity.
RECA_ENAn	59	TRIOD6	SSR Enable for Serial REC of A Port.
RECA_RDY	71	IN	SSR Ready for Serial REC of A Port.
PBA_DATA	51	IN	SSR Serial PB of A Port.
PBA_CLK	57	TRIOD6	SSR Clock for Serial PB of A Port.
PBA_CLKn	55	TRIOD6	SSR Clock for Serial PB of A Port in reverse polarity.
PBA_ENAn	50	TRIOD6	SSR Enable for Serial PB of A Port.
PBA_RDY	58	IN	SSR Ready for Serial PB of A Port.
TLMA_DATA	39	IN	SSR Serial ST of A Port.
TLMA_CLK	46	TRIOD6	SSR Clock for Serial ST of A Port.
TLMA_CLKn	43	TRIOD6	SSR Clock for Serial ST of A Port in reverse polarity.
TLMA_ENAn	41	TRIOD6	SSR Enable for Serial ST of A Port.
TLMA_RDY	49	IN	SSR Ready for Serial ST of A Port.
CMDB_DATA	30	TRIOD6	SSR Serial CMD of B Port.
CMDB_DATAn	35	TRIOD6	SSR Serial CMD of B Port in reverse polarity.
CMDB_CLK	33	TRIOD6	SSR Clock for Serial CMD of B Port.
CMDB_CLKn	32	TRIOD6	SSR Clock for Serial CMD of B Port in reverse polarity.
CMDB_ENAn	38	TRIOD6	SSR Enable for Serial CMD of B Port.
CMDB_RDY	37	IN	SSR Ready for Serial CMD of B Port.
RECB_DATA	28	TRIOD6	SSR Serial REC of B Port.
RECB_DATAn	29	TRIOD6	SSR Serial REC of B Port in reverse polarity.
RECB_CLK	23	TRIOD6	SSR Clock for Serial REC of B Port.
RECB_CLKn	20	TRIOD6	SSR Clock for Serial REC of B Port in reverse polarity.
RECB_ENAn	27	TRIOD6	SSR Enable for Serial REC of B Port.
RECB_RDY	26	IN	SSR Ready for Serial REC of B Port.
PBB_DATA	16	IN	SSR Serial PB of B Port.
PBB_CLK	10	TRIOD6	SSR Clock for Serial PB of B Port.
PBB_CLKn	8	TRIOD6	SSR Clock for Serial PB of B Port in reverse polarity.
PBB_ENAn	17	TRIOD6	SSR Enable for Serial PB of B Port.
PBB_RDY	13	IN	SSR Ready for Serial PB of B Port.

⁵ The pin numbers of bus signals are in the same sequence as the signals.

⁶ For a description of the signal type refer to Table 4-9.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY		
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A	
SHEET 11			SHEET 11	

Table 2-1. Signal Descriptions (Cont'd)

Name	Pin No. ⁷	Type ⁸	Description
TLMB_DATA	11	IN	SSR Serial ST of B Port.
TLMB_CLK	4	TRIOD6	SSR Clock for Serial ST of B Port.
TLMB_CLKn	253	TRIOD6	SSR Clock for Serial ST of B Port in reverse polarity.
TLMB_ENAn	12	TRIOD6	SSR Enable for Serial ST of B Port.
TLMB_RDY	7	IN	SSR Ready for Serial ST of B Port.
Rigel ⁹	247	INPD	Rigel test command. Forces internal logic to assume functionality compatible with the Rigel test vector generation tool.
TCK ⁹	249	INPD	Test Circuitry Clock.
TDI ⁹	246	INPU	Test Data In. Serial data in for scan path test logic.
TMS ⁹	252	INPU	Test Mode Select. Commands the scan logic mode.
TRSTN ⁹	251	INPU	Test Reset. Forces all nodes visible to the scan paths to a known state for test purposes; not necessarily the same state values as nPOR.
TDO ⁹	245	TRI6	Test Output Data. Serial bit stream from the internal scan paths.
PWR	1, 65, 129, 193	VDD	Vdd Power Pads.
GND	2, 63, 64, 66, 127, 128, 130, 191, 192, 194, 255, 256	VSS	Vss Power Pads.

⁷ The pin numbers of bus signals are in the same sequence as the signals.

⁸ For a description of the signal type refer to Table 4-9.

⁹ These signals are defined for use with the Honeywell On-Chip Monitor (OCM) scan path control block, and their Rigel test vector generator. See Honeywell manuals for precise definitions of these signals. These signals are not expected to be used in flight hardware.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 12		SHEET 12	

3. FUNCTIONAL DESCRIPTION

3.1 Functional Overview

Figure 3-1 contains a block diagram of the SSRIU. The arrows in the block diagram indicate the direction on data flow. Note that for the Command Interface and Record Interface, commands and data flow from SSRIU to the SSR. For the Playback Interface and Status Interface the direction of data flow is the opposite, data flows from the SSR to the SSRIU.

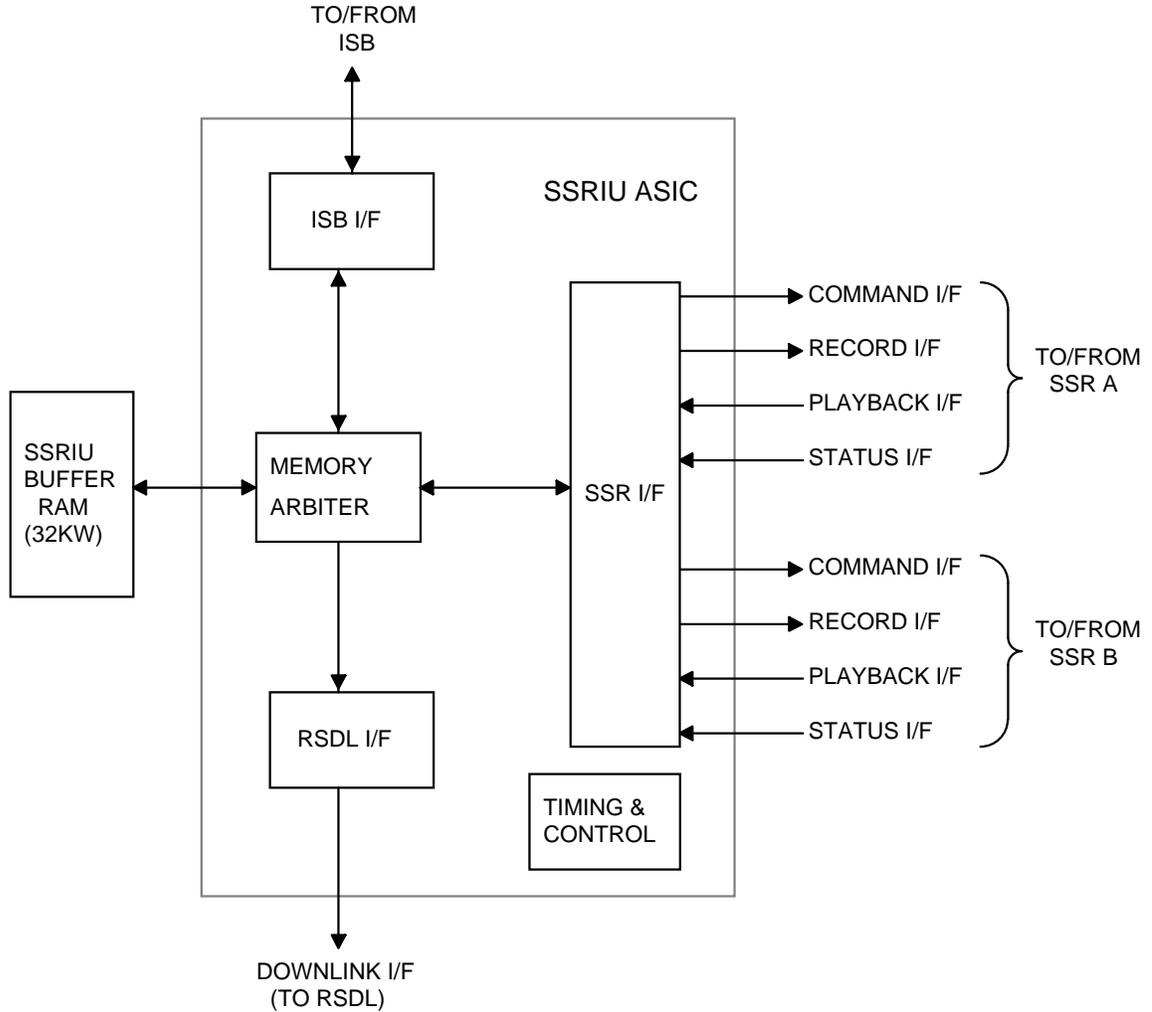


Figure 3-1. SSRIU Block Diagram

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 13			SHEET 13

3.2 SSRIU Interfaces

The SSRIU's main function is to provide the FSW with the five interfaces: a Downlink Interface, and four SSR interfaces: SSR Command Interface, SSR Record Interface, SSR Playback Interface, and SSR Status Interface. The Command I/F is used by FSW to send commands to the SSR. The Record I/F is used by FSW to record data on the SSR. The Playback I/F is used by FSW to read data from the SSR. The Status I/F is used by FSW to read status from the SSR. It is important to note that these five interfaces operate independently. Transactions may take place on all five interfaces simultaneously.

3.3 SSRIU Buffers

The FSW interacts with these five interfaces via six buffers (there are two buffers associated with the Downlink Interface, and one buffer for each on the remaining interfaces). These six buffers all reside within the same 32kw of buffer RAM. The start address and end address of each buffer is specified by FSW in SSRIU registers. All of the buffers are accessible via the ISB. Each data buffer is summarized below:

3.3.1 SSR Command Buffer

FSW can send commands to the SSR by loading this buffer with SSR commands via the ISB and then setting the appropriate "Go" bit in Register 0. The SSRIU will then autonomously send the contents of the Command Buffer to the SSR via the Command I/F. When the transfer is complete, the SSRIU sets a status bit in Register 2 and asserts an interrupt (if the interrupt is unmasked).

3.3.2 SSR Record Buffer

FSW can record data on the SSR by loading this buffer with the data via the ISB and then setting the appropriate "Go" bit in Register 0. The SSRIU will then autonomously send the contents to the Record Buffer to the SSR via the Record I/F. When the transfer is complete, the SSRIU sets a status bit in Register 2 and asserts an interrupt (if the interrupt is unmasked).

3.3.3 SSR Playback Buffer

FSW can read data from the SSR by setting the appropriate "Go" bit in Register 0. The SSRIU then autonomously reads data from the SSR via the Playback Interface and places it in the Playback Buffer. When the end of the buffer is reached, the transfer is complete, and the SSRIU sets a status bit in Register 2 and asserts an interrupt (if the interrupt is unmasked).

3.3.4 SSR Status Buffer

FSW can read status from the SSR by setting the appropriate "Go" bit in Register 0. The SSRIU then autonomously reads status from the SSR via the Status Interface and places it in the Status Buffer. When the end of the buffer is reached, the transfer is complete, and the SSRIU sets a status bit in Register 2 and asserts an interrupt (if the interrupt is unmasked).

3.3.5 Downlink Buffers A and B

W can send either real time data or SSR playback data to the downlink by using Downlink (DL) Buffers A and B. FSW can load real time data into the DL Buffers via the ISB. SSR playback data can be loaded into a DL Buffer by setting the start and end addresses for the Playback Buffer and the DL Buffer the same. The RSDL continuously

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 14			SHEET 14

reads data from one of the DL Buffers and sends it to the downlink. FSW can select which buffer data is read from via RSDL registers.

3.4 SSRIU Timing

All four SSRIU-SSR interfaces are synchronous interfaces with the SSRIU initiating a transaction by asserting the ENABLE signal. The SSR then responds by asserting the READY signal. The SSRIU then starts sending a 1.5 MHz clock to the SSR. Multiple 16-bit words may be transferred during a single assertion of the ENABLE signal. The timing diagram for the Command I/F is shown below.

3.4.1 Command Interface Timing

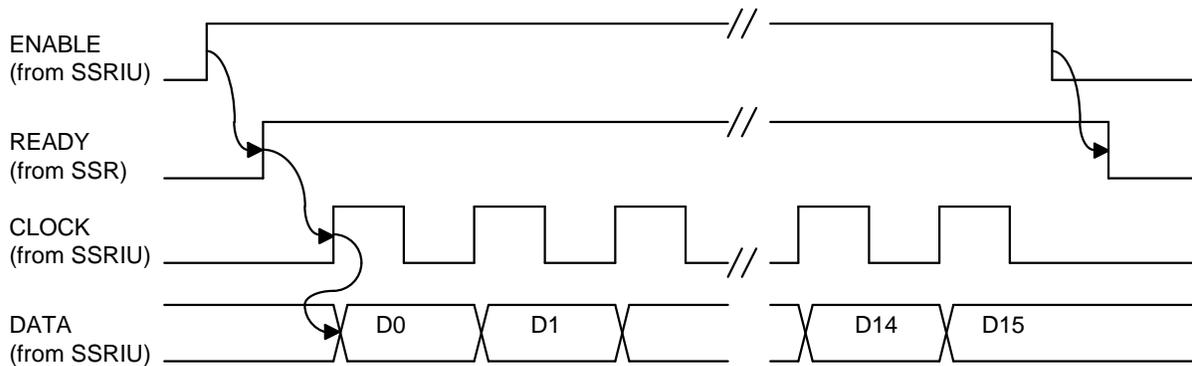


Figure 3-2. SSRIU Command Interface Timing Diagram

3.4.2 Record Interface Timing

The SSRIU Record I/F timing diagram is shown in Figure 3-3. On the Record I/F, if the SSR is having trouble keeping up with the data flow it can temporarily halt the data flow by negating the READY signal. At the end of the next word, the SSRIU will stop sending data to the SSR. When the SSR is once again ready for more data, it asserts the READY signal and the SSRIU once again starts sending data to the SSR, continuing where it left off. This is the main difference between the Record I/F timing and the Command I/F timing.

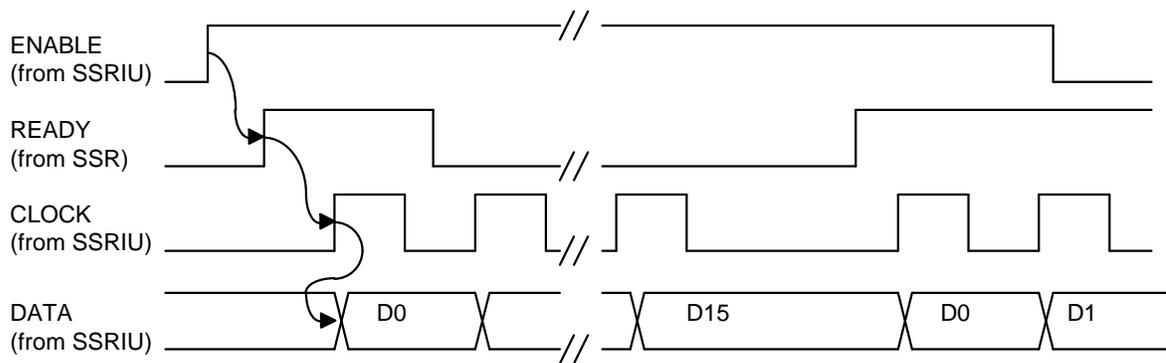


Figure 3-3. SSRIU Record Interface Timing Diagram

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SHEET 15			SHEET 15

3.4.3 Playback Interface Timing

The SSRIU Playback I/F timing diagram is shown in Figure 3-4. It is identical to that of the Record I/F with one exception; data is now being sourced by the SSR. Note, however, that the SSRIU still supplies the clock.

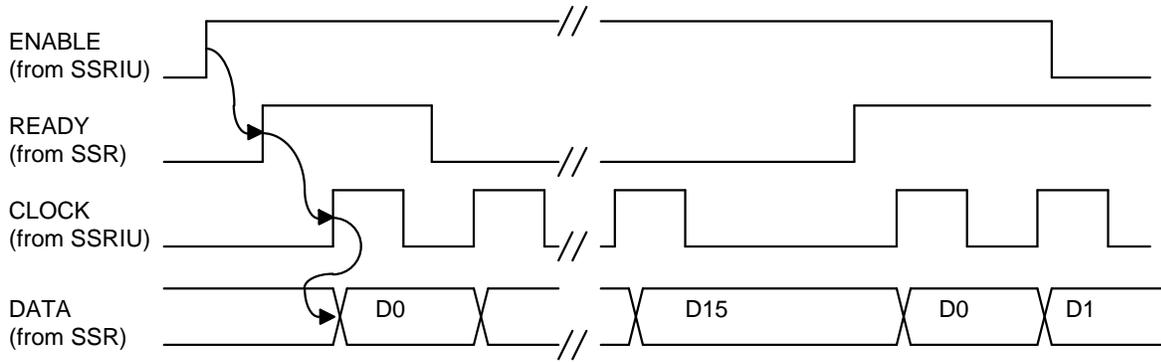


Figure 3-4. SSRIU Playback Interface Timing Diagram

3.4.4 Status Interface Timing

The SSRIU Status I/F timing diagram is shown in Figure 3-5. It is identical to that of the Record I/F with one exception; data is now being sourced by the SSR. Note, however, that the SSRIU still supplies the clock.

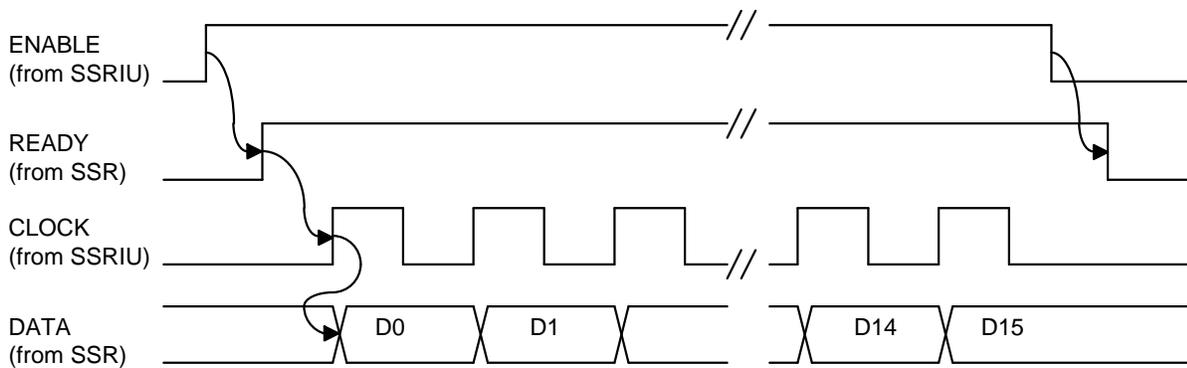


Figure 3-5. SSRIU Status Interface Timing Diagram

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 16		SHEET 16	

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical Test Requirements

Test	Subgroups (Per MIL-STD-883, Method 5005, Table 1)
Initial (Pre Burn-In)	1,7
Interim (Post Static I Burn-In)	1*,7*
Delta Calculations*,**	
Interim (Post Static II Burn-In)	1*,7*
Delta Calculations*,**	
Final (Post Dynamic Burn-In)	1*,2,3,7*,8,9,10,11
Delta Calculations*,**	
Group A	1,2,3,7,8,9,10,11
Group C End Point electrical***	1,2,3,7,8,9,10,11
Delta Calculations**	

Table 4-1. Electrical Test Requirements

- * PDA applies to these subgroups
- ** Deltas shall be calculated relative to the initial electrical parameters. Delta limits of Table 4-8 herein shall apply.
- *** Group C Lifetest shall be performed using the dynamic burn-in configuration of Table 4-7 herein.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 17			SHEET 17

4.2 Absolute Maximum Ratings ^{10,11,12}

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V _{DD}	Supply Voltage	-0.5	7.0	V
V _{IN}	Input Voltage Range	GND - 0.5	V _{DD} + 0.5	V
I _{OUT}	DC Output Current (per Output)		50	mA
P _D	Max. Package Power Dissipation		4	W
T _{ST}	Storage Temperature Range	-65	150	°C
T _S	Lead Temperature (Soldering, 5s)		270	°C
T _J	Junction Temperature		175	°C
Θ _{JC}	Thermal Resistance, Junction to Case		4	°C/W
V _{ESD}	ESD Protection Voltage - Class 2 (MIL-STD-883, Method 3015)	2000		V

Table 4-2. Absolute Maximum Ratings

4.3 Recommended Operating Conditions ^{12,13}

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V _{DD}	Supply Voltage	4.5	5.5	V
T _A	Ambient Temperature	-55	125	°C
f _{max}	Max. Operating Frequency		12	MHz
t _r , t _f	Input Rise Time, Input Fall Time		500	ns

Table 4-3. Recommended Operating Conditions.

¹⁰ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and effect reliability.

¹¹ Values are guaranteed but not tested.

¹² -55°C ≤ T_C ≤ 125°C except as noted.

¹³ Extended operation outside recommended limits may degrade performance and effect reliability.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 18		SHEET 18	

4.4 DC Characteristics

4.4.1 DC Electrical Performance Characteristics

Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Input Threshold Voltage	V_{IH}	$V_{DD}=5.5V$	1,2,3		3.85	V
	V_{IL}	$V_{DD}=4.5V$	1,2,3	1.35		V
Input Leakage Current	I_{IH1}^{14}	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	-10	10	μA
	I_{IH2}^{15}	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	-10	10	μA
	I_{IH3}^{16}	$V_{DD}=5.5V, V_{IH}=V_{DD}$	1,2,3	50	550	μA
	I_{IL1}^{14}	$V_{DD}=5.5V, V_{IL}=GND$	1,2,3	-10	10	μA
	I_{IL2}^{15}	$V_{DD}=5.5V, V_{IL}=GND$	1,2,3	-550	-50	μA
	I_{IL3}^{16}	$V_{DD}=5.5V, V_{IL}=GND$	1,2,3	-10	10	μA
Output Leakage Current (Tristate)	I_{OZH}	$V_{DD}=5.5V, V_O=V_{DD}$	1,2,3	-10	10	μA
	I_{OZL}	$V_{DD}=5.5V, V_O=GND$	1,2,3	-10	10	μA
Output Voltage	V_{OH}	$V_{DD}=4.5V, I_{OH}=-6mA$	1,2,3	4.0		V
	V_{OL}	$V_{DD}=4.5V, I_{OL}=6mA$	1,2,3		0.5	V
Output Current	I_{OH}	$V_{DD}=4.5V, V_{OH}=4.0V$	1,2,3		-6	mA
	I_{OL}	$V_{DD}=4.5V, V_{OL}=0.5V$	1,2,3	6		mA
Standby Supply Current	I_{DDSB}	$V_{DD}=5.5V, V_{IN}=V_{DD}$ or GND, $F_c=0$ Hz	1,2,3		800	μA
Quiescent Current	I_{DDQ}	$V_{DD}=5.5V, V_{IN}=V_{DD}$ or GND, $F_c=0$ Hz	1		5	μA
Operating Current	I_{DDOP}^{17}	$V_{DD}=5.5V, V_{IN}=V_{DD}$ or GND, $F_c=12$ MHz	1,2,3		100	mA
Input Capacitance ¹⁸	C_{IN}				15	pF
Output Capacitance ^{18,19}	C_{OUT}				15	pF

Table 4-4. DC Performance Characteristics

¹⁴ All Inputs, except: TDI, TMS, TRSTN, TCK, Rigel, M11.9_CLK.

¹⁵ Inputs with Pull-Ups: TDI, TMS, TRSTN.

¹⁶ Inputs with Pull-Downs: TCK, Rigel, M11.9_CLK.

¹⁷ This value is based on the supplied functional test vector set and the ANDO tester loading (85 pF) and may not be applicable to system operation.

¹⁸ Guaranteed but not tested.

¹⁹ Refers to internal capacitance.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY			
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)		ST 12169	REV. A
SHEET 19				SHEET 19	

4.4.2 Estimated Power Dissipation.

$$P_{\text{Total}} = P_{\text{Internal}} + P_{\text{Outputs}} + P_{\text{Quiescent}} = 340.3 + 27.7 + 4.4 = 372.4 \text{ mW}$$

$$P_{\text{Internal}} = \frac{1}{2} * f_{\text{CLK}} * C_{\text{Lint}} * (V_{\text{DD}})^2 = 340.3 \text{ mW}$$

Where:

C_{Lint}	=	$S * \text{\#of Nets} * 0.75\text{pf}$
S	=	0.25
\#of Nets	=	10,000
f_{CLK}	=	12 MHz
V_{DD}	=	5.5V

$$P_{\text{Outputs}} = \frac{1}{2} * f_{\text{CLK}} * C_{\text{Lout}} * (V_{\text{DD}})^2 + P_{\text{Crowbar}} = 25.2 + 2.5 = 27.7 \text{ mW}$$

Where:

C_{Lout}	=	$S * \text{\#of Output Pads} * 50 (25) \text{ pf}$
S	=	0.04
\#of Output Pads	=	33 @ 50 pF 73 @ 25 pF
f_{CLK}	=	12 MHz
V_{DD}	=	5.5V
P_{Crowbar}	=	10% of P_{Outputs}

$$P_{\text{Quiescent}} = V_{\text{DD}} * I_{\text{DDSB}} = 4.4 \text{ mW}$$

Where:

V_{DD}	=	5.5V
I_{DDSB}	=	800 μA

4.4.3 IDDQ Testing.

Quiescent Current (IDDQ) testing shall be accomplished by using the Stuck-at Fault test vectors generated with RIGEL, or a subset thereof, as determined by JPL. Measurements shall be taken at every vector, unless otherwise indicated, recorded and compared to the IDDQ limit. The following statistical values shall be provided: Minimum, Maximum, Mean, Standard Deviation. The IDDQ limits shall be established by JPL after characterization of Engineering Model parts which are fabricated from the same wafer lot as the flight parts.

4.4.4 Pulldown Resistors.

The internal pulldown resistor design option has been used on the following input pads:

TCK
Rigel
M11.9_CLK

It is recommended that the TCK and Rigel signals be tied low (logic 0) in the flight hardware.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 20		SHEET 20	

4.4.5 Pullup Resistors.

The internal pullup resistor design option has been used on the following input pads:

TDI
TMS
TRSTN

It is recommended that the TDI and TMS signals be tied high (logic 1) in the flight hardware. TRSTN must be held low during power-up and therefore is recommended to be tied low (logic 0).

4.4.6 Open Drain Outputs.

Following Tristate Outputs are configured as Open Drain outputs:

CMDA_DATA	RECA_DATA		
CMDA_DATAn	RECA_DATAn		
CMDA_CLK	RECA_CLK	PBA_CLK	TLMA_CLK
CMDA_CLKn	RECA_CLKn	PBA_CLKn	TLMA_CLKn
CMDA_ENAn	RECA_ENAn	PBA_ENAn	TLMA_ENAn
CMDB_DATA	RECB_DATA		
CMDB_DATAn	RECB_DATAn		
CMDB_CLK	RECB_CLK	PBB_CLK	TLMB_CLK
CMDB_CLKn	RECB_CLKn	PBB_CLKn	TLMB_CLKn
CMDB_ENAn	RECB_ENAn	PBB_ENAn	TLMB_ENAn

DC parameters V_{OH} and I_{OH} for these Open Drain outputs can be measured by utilizing the serial scan to set the Open Drain outputs to a High state during test.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 21			SHEET 21

4.5 AC Characteristics

4.5.1 AC Electrical Performance Characteristics

Parameter	Symbol	Test Condition $V_{IN}=V_{DD}$ or GND	Subgroup	Specification Limit		Tester Limit ^{20,21}		Unit
				Min	Max	Min	Max	
Functional Tests		$V_{DD}=4.5$ & $5.5V$ $F_c=1$ MHz	7,8	pass		pass		
Propagation Delay:		$V_{DD}=4.5$ & $5.5V$ $F_c=500$ kHz						
M11.9_CLK to DTACKN	t_{PLH1} t_{PHL1}		9,10,11	6 5	39 39	6.0 5.0	37.4 37.0	ns ns
M11.9_CLK to MEMOEN	t_{PLH2} t_{PHL2}		9,10,11	6 6	39 40	6.0 6.0	37.4 38.0	ns ns
M11.9_CLK to D(15:0), DP	t_{PZH1} t_{PZL1}		9,10,11	11 10	57 56	11.0 10.0	52.9 51.0	ns ns
Set-up Time:		$V_{DD}=4.5$ & $5.5V$ $F_c=500$ kHz						
RDECODE to M11.9_CLK	t_{SU1}		9,10,11		23		23.0	ns
MDECODE to M11.9_CLK	t_{SU2}		9,10,11		22		22.0	ns
Hold Time:		$V_{DD}=4.5$ & $5.5V$ $F_c=500$ kHz						
M11.9_CLK to RDECODE	t_{HD1}		9,10,11		4		4.0	ns
M11.9_CLK to MDECODE	t_{HD2}		9,10,11		4		4.0	ns

Table 4-5. AC Performance Characteristics

4.5.2 Timing Analysis.

Pre-layout and post-layout timing shall pass the QuickSim simulation of the vectors supplied to the contractor without setup/hold timing violations.

4.5.2.1 Pre-Layout Timing Margins.

Pre-layout timing margins shall be calculated by using standard extreme-value analysis. The extreme values for the cell library shall be supplied by the contractor. Critical paths will be identified and margin calculated via Mentor or Honeywell software toolsets, or a combination thereof.

²⁰ Tester limits are shown from a test perspective (i.e., set-up time, hold time are shown as max. limits).

²¹ Tester limits do not include guardbanding for tester errors.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY			
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)		ST 12169	REV. A
SHEET 22		SHEET 22			

4.5.2.2 Post-Layout Timing Margins.

Post-layout analysis of the device shall show positive margin on internal critical paths over all operating conditions. The analysis will follow the same form as the pre-layout analysis, with the post-layout timing values annotated to the design file by the contractor.

4.5.2.3 Tester Specification Limits.

Tester limits in Table 4-5 have been adjusted for modified output levels and for differences in output loading in the ANDO tester environment. Modified output levels are required to account for impedance mismatches between device outputs and the ANDO tester environment. The level at which an output is considered to have switched has been changed from 50% of VDD to 1V for low to high transitions and VDD-0.5V for high to low transitions for the 3mA buffer and to 1V for low to high transitions and VDD-1V for high to low transitions for the higher drive buffers (6mA, 9mA, 12mA, 15mA).

$$t_{SPEC}(Tester) = t_{SPEC}(System) - (T_{Offset_fixed} + C_{Load} * LoadingFactor)$$

Where:

$$C_{Load} (System Simulation) = 25 \text{ pF} - DTACKN, MEMOEN$$

$$50 \text{ pF} - D(15-0)$$

For 6 mA drive buffer:

Low to High transition:	$T_{Offset_fixed} = -1.0 \text{ ns}$	LoadingFactor = 0.103
High to Low transition:	$T_{Offset_fixed} = -1.0 \text{ ns}$	LoadingFactor = 0.121

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY		
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169	REV. A
SHEET 23			SHEET 23	

4.5.3 Tester Load Circuit

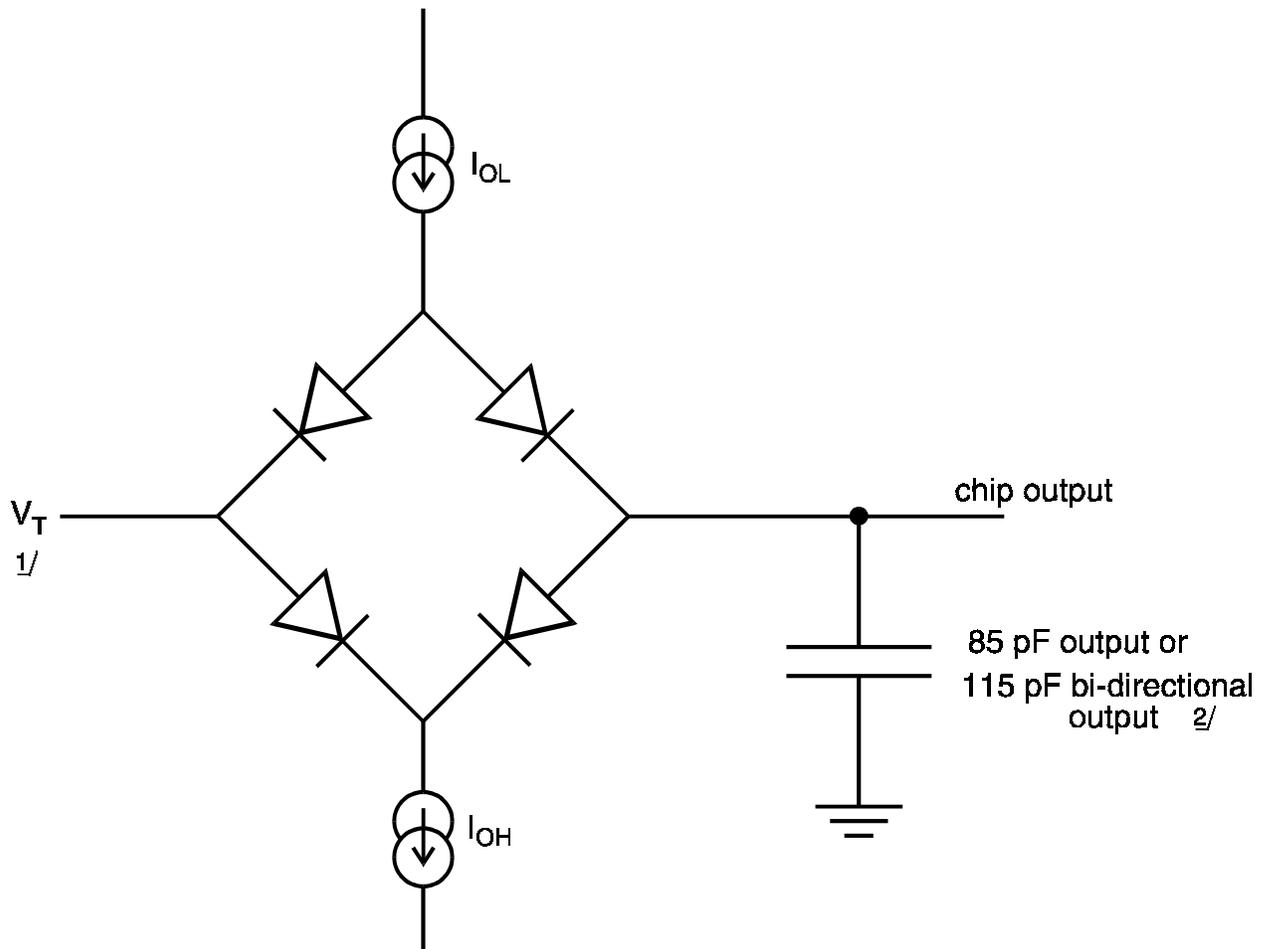


Figure 4-1. Tester Load Circuit

1/ V_T is a variable dependent upon the test parameter.

2/ This capacitance is actually partially distributed through the fixturing so that the device is actually loaded by a transmission line.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 24			SHEET 24

4.6 Burn-In

4.6.1 Static Burn-In

The Static Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7.

4.6.2 Dynamic Burn-In

The Dynamic Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7. Input stimuli (STIM) to exercise the device shall be applied by using the RIGEL Stuck-at Fault test vectors, or a subset thereof, as determined by JPL. At least one output (MON) shall be monitored during burn-in to assure that the output is toggled and the circuit functioning.

4.6.3 Burn-In Conditions

	Static I	Static II	Dynamic	QCI - Life Test
Duration	48 hours	48 hours	240 hours	2000 hours
Voltage	6.5 V	6.5 V	6.5 V	6.0 V
+ Tolerance	+0.1V	+0.1V	+0.1V *	+0.1V *
- Tolerance	-0.25V	-0.25V	-0.25V	-0.25V
Temperature	125 °C	125 °C	125 °C	125 °C
+ Tolerance	+5 °C	+5 °C	+5 °C	+5 °C
- Tolerance	-0 °C	-0 °C	-0 °C	-0 °C

Table 4-6. Burn-In Conditions

* Applies to Average Power Supply Voltage. Tolerance for Dynamic Switching Noise is +0.25V.

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY	
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 25			SHEET 25

4.6.4 Burn-In Configuration

Pin Name	Pin No. ²²	Type ²³	Burn-In Test Connection ²⁴			Description
			Static I	Static II	Dynamic	
A(14:0)	173, 174, 177, 181, 187, 198, 201, 204, 210, 216, 222, 225, 226, 229, 234	IN	GND	VDD	VDD	ISB Address Bus (32KW).
DP	231	BI6	GND	VDD	VDD	ISB Data Parity.
D(15:0)	176, 180, 183, 186, 189, 197, 200, 203, 206, 209, 212, 215, 218, 221, 224, 228	BI6	GND	VDD	VDD	ISB Data Bus.
DPE _n	233	OUT6	GND	VDD	VDD	ISB Data Parity Error.
ARE _n	248	OUT6	GND	VDD	VDD	ISB Address Range Error.
ADV _n	236	IN	GND	VDD	VDD	ISB Address Valid.
RDIR	235	IN	GND	VDD	VDD	ISB Read Direction.
DTACK _n	243	OUT6	GND	VDD	VDD	ISB Data Transfer Acknowledge.
SSRIU_INT _n	6	OUT6	GND	VDD	VDD	SSRIU interrupt line.
MDECODE	241	IN	GND	VDD	VDD	Select Local Memory.
RDECODE	242	IN	GND	VDD	VDD	Select Local Register.
M11.9_CLK	238	INPD	GND	VDD	VDD	11.9448MHZ clock .
MEMA(14:0)	94, 95, 98, 101, 107, 110, 113, 118-120, 123, 134, 137, 138, 141	OUT6	GND	VDD	VDD	SSR/DL Memory Buffer Address Bus.
MEMD(15:0)	90, 93, 97, 100, 103, 106, 109, 112, 115, 117, 122, 125, 133, 136, 140, 144	BI6	GND	VDD	VDD	SSR/DL Memory Buffer Data Bus.
MEMCS _n	86	OUT6	GND	VDD	VDD	SSR/DL Memory Buffer Chip Select.
MEMWE _n	88	OUT6	GND	VDD	VDD	SSR/DL Memory Buffer Write Enable.
MEMOE _n	87	OUT6	GND	VDD	VDD	SSR/DL Memory Buffer Output Enable.
BUFSEL	152	IN	GND	VDD	VDD	Buffer Select for the DL buffer.
BUFSWAP	76	IN	GND	VDD	VDD	Swap the DL buffer.

Table 4-7. Burn-In Configuration

²² The pin numbers of bus signals are in the same sequence as the signals.

²³ For a description of the signal type refer to Table 4-9.

²⁴ All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY			
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)		ST 12169	REV. A
SHEET 26				SHEET 26	

Pin Name	Pin No. ²⁵	Type ²⁶	Burn-In Test Connection ²⁷			Description
			Static I	Static II	Dynamic	
EOB	169	OUT6	GND	VDD	VDD	End of the DL buffer.
RSTn	240	IN	GND	VDD	VDD	Synchronous Reset.
DLREQn	171	IN	GND	VDD	VDD	DL request.
DLDONEn	168	OUT6	GND	VDD	VDD	DL request has been served.
DLDATA(15:0)	145-147, 150, 151, 153, 154, 158-165, 170	OUT6	GND	VDD	VDD	DL Data bus.
SSRAn	52	IN	GND	VDD	VDD	Select SSR A or B Port.
HEALTH	67	IN	GND	VDD	VDD	CDS Health.
CMDA_DATA	74	TRIOD6	GND	VDD	VDD	SSR Serial CMD of A Port.
CMDA_DATAAn	75	TRIOD6	GND	VDD	VDD	SSR Serial CMD of A Port in reverse polarity.
CMDA_CLK	80	TRIOD6	GND	VDD	VDD	SSR Clock for Serial CMD of A Port.
CMDA_CLKn	77	TRIOD6	GND	VDD	VDD	SSR Clock for Serial CMD of A Port in reverse polarity.
CMDA_ENAn	84	TRIOD6	GND	VDD	VDD	SSR Enable for Serial CMD of A Port.
CMDA_RDY	83	IN	GND	VDD	VDD	SSR Ready for Serial CMD of A Port.
RECA_DATA	73	TRIOD6	GND	VDD	VDD	SSR Serial REC of A Port.
RECA_DATAAn	72	TRIOD6	GND	VDD	VDD	SSR Serial REC of A Port in reverse polarity.
RECA_CLK	68	TRIOD6	GND	VDD	VDD	SSR Clock for Serial REC of A Port.
RECA_CLKn	62	TRIOD6	GND	VDD	VDD	SSR Clock for Serial REC of A Port in reverse polarity.
RECA_ENAn	59	TRIOD6	GND	VDD	VDD	SSR Enable for Serial REC of A Port.
RECA_RDY	71	IN	GND	VDD	VDD	SSR Ready for Serial REC of A Port.
PBA_DATA	51	IN	GND	VDD	VDD	SSR Serial PB of A Port.
PBA_CLK	57	TRIOD6	GND	VDD	VDD	SSR Clock for Serial PB of A Port.

Table 4-7. Burn-In Configuration (Cont'd)

²⁵ The pin numbers of bus signals are in the same sequence as the signals.

²⁶ For a description of the signal type refer to Table 4-9.

²⁷ All inputs and outputs shall be tied to the specified voltage level through a 2.2 k Ω resistor ($\pm 5\%$, 1/4W).

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY				
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)			ST 12169	REV. A
SHEET 27					SHEET 27	

Pin Name	Pin No. ²⁸	Type ²⁹	Burn-In Test Connection ³⁰			Description
			Static I	Static II	Dynamic	
PBA_CLKn	55	TRIOD6	GND	VDD	VDD	SSR Clock for Serial PB of A Port in reverse polarity.
PBA_ENAn	50	TRIOD6	GND	VDD	VDD	SSR Enable for Serial PB of A Port.
PBA_RDY	58	IN	GND	VDD	VDD	SSR Ready for Serial PB of A Port.
TLMA_DATA	39	IN	GND	VDD	VDD	SSR Serial ST of A Port.
TLMA_CLK	46	TRIOD6	GND	VDD	VDD	SSR Clock for Serial ST of A Port.
TLMA_CLKn	43	TRIOD6	GND	VDD	VDD	SSR Clock for Serial ST of A Port in reverse polarity.
TLMA_ENAn	41	TRIOD6	GND	VDD	VDD	SSR Enable for Serial ST of A Port.
TLMA_RDY	49	IN	GND	VDD	VDD	SSR Ready for Serial ST of A Port.
CMDB_DATA	30	TRIOD6	GND	VDD	VDD	SSR Serial CMD of B Port.
CMDB_DATAn	35	TRIOD6	GND	VDD	VDD	SSR Serial CMD of B Port in reverse polarity.
CMDB_CLK	33	TRIOD6	GND	VDD	VDD	SSR Clock for Serial CMD of B Port.
CMDB_CLKn	32	TRIOD6	GND	VDD	VDD	SSR Clock for Serial CMD of B Port in reverse polarity.
CMDB_ENAn	38	TRIOD6	GND	VDD	VDD	SSR Enable for Serial CMD of B Port.
CMDB_RDY	37	IN	GND	VDD	VDD	SSR Ready for Serial CMD of B Port.
RECB_DATA	28	TRIOD6	GND	VDD	VDD	SSR Serial REC of B Port.
RECB_DATAn	29	TRIOD6	GND	VDD	VDD	SSR Serial REC of B Port in reverse polarity.
RECB_CLK	23	TRIOD6	GND	VDD	VDD	SSR Clock for Serial REC of B Port.
RECB_CLKn	20	TRIOD6	GND	VDD	VDD	SSR Clock for Serial REC of B Port in reverse polarity.
RECB_ENAn	27	TRIOD6	GND	VDD	VDD	SSR Enable for Serial REC of B Port.
RECB_RDY	26	IN	GND	VDD	VDD	SSR Ready for Serial REC of B Port.
PBB_DATA	16	IN	GND	VDD	VDD	SSR Serial PB of B Port.
PBB_CLK	10	TRIOD6	GND	VDD	VDD	SSR Clock for Serial PB of B Port.
PBB_CLKn	8	TRIOD6	GND	VDD	VDD	SSR Clock for Serial PB of B Port in reverse polarity.
PBB_ENAn	17	TRIOD6	GND	VDD	VDD	SSR Enable for Serial PB of B Port.
PBB_RDY	13	IN	GND	VDD	VDD	SSR Ready for Serial PB of B Port.

Table 4-7. Burn-In Configuration (Cont'd)

²⁸ The pin numbers of bus signals are in the same sequence as the signals.

²⁹ For a description of the signal type refer to Table 4-9.

³⁰ All inputs and outputs shall be tied to the specified voltage level through a 2.2 k Ω resistor ($\pm 5\%$, 1/4W).

JET PROPULSION LABORATORY		CALIFORNIA INSTITUTE OF TECHNOLOGY			
ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)		ST 12169	REV. A
SHEET 28				SHEET 28	

Pin Name	Pin No. ³¹	Type ³²	Burn-In Test Connection ³³			Description
			Static I	Static II	Dynamic	
TLMB_DATA	11	IN	GND	VDD	VDD	SSR Serial ST of B Port.
TLMB_CLK	4	TRIOD6	GND	VDD	VDD	SSR Clock for Serial ST of B Port.
TLMB_CLKn	253	TRIOD6	GND	VDD	VDD	SSR Clock for Serial ST of B Port in reverse polarity.
TLMB_ENAn	12	TRIOD6	GND	VDD	VDD	SSR Enable for Serial ST of B Port.
TLMB_RDY	7	IN	GND	VDD	VDD	SSR Ready for Serial ST of B Port.
Rigel	247	INPD	GND	VDD	STIM ³⁴	Rigel test command.
TCK	249	INPD	GND	VDD	STIM ³⁴	Test Circuitry Clock.
TDI	246	INPU	GND	VDD	STIM ³⁴	Test Data In.
TMS	252	INPU	GND	VDD	STIM ³⁴	Test Mode Select
TRSTN	251	INPU	GND	VDD	STIM ³⁴	Test Reset
TDO	245	TRI6	GND	VDD	MON ³⁵	Test Output Data
PWR	1, 65, 129, 193	VDD	6.5V	6.5V	6.5V (6V for Lifetest)	Vdd Power Pads.
GND	2, 63, 64, 66, 127, 128, 130, 191, 192, 194, 255, 256	VSS	0.0V	0.0V	0.0V	Vss Power Pads.

Table 4-7. Burn-In Configuration (Cont'd)

³¹ The pin numbers of bus signals are in the same sequence as the signals.

³² For a description of the signal type refer to Table 4-9.

³³ All inputs and outputs shall be tied to the specified voltage level through a 2.2 k Ω resistor ($\pm 5\%$, 1/4W).

³⁴ Stimulated Input

³⁵ Monitored Output

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)			ST 12169 REV. A
SHEET 29					SHEET 29

4.6.5 Delta Limits

Symbol	Parameter	Spec. Limits		Units	Delta Limits	Units
		Min	Max			
I _{DDSB}	Static Supply Current		800	μA	80	μA
I _{IL1} ³⁶	Input Leakage Current Low	-10	10	μA	±1	μA
I _{IL2} ³⁷	Input Leakage Current Low, Pull-Ups	-550	-50	μA	±55	μA
I _{IL3} ³⁸	Input Leakage Current Low, Pull-Downs	-10	10	μA	±1	μA
I _{IH1} ³⁷	Input Leakage Current High	-10	10	μA	±1	μA
I _{IH2} ³⁸	Input Leakage Current High, Pull-Ups	-10	10	μA	±1	μA
I _{IH3} ³⁹	Input Leakage Current High, Pull-Downs	50	550	μA	±55	μA
I _{OZL}	Output Leakage Current Low	-10	10	μA	±1	μA
I _{OZH}	Output Leakage Current High	-10	10	μA	±1	μA
I _{OL}	Output Current Low		6	mA	±600	μA
I _{OH}	Output Current High	-6		mA	±600	μA

Table 4-8. Delta Limits

4.7 Pin Type Description

Pin Name	Drive	I/O	Type
IN	=	CMOS,	Input Signal
INPU	=	CMOS,	Input Signal with Pull-up
INPD	=	CMOS,	Input Signal with Pull-down
TRI6	= 6mA,	CMOS,	Tri-State Signal
TRIOD6	= 6mA,	CMOS,	Tri-State Signal, Open Drain Outputs
OUT6	= 6mA,	CMOS,	Output Signal
BI6	= 6mA,	CMOS,	Bidirectional Signal

Table 4-9. Pin Type Description

³⁶ All Inputs, except: TDI, TMS, TRSTN, TCK, Rigel, M11.9_CLK.

³⁷ Inputs with Pull-Ups: TDI, TMS, TRSTN.

³⁸ Inputs with Pull-Downs: Rigel, M11.9_CLK.

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 30		SHEET 30	

5. PHYSICAL CHARACTERISTICS

5.1 Pin Assignment.

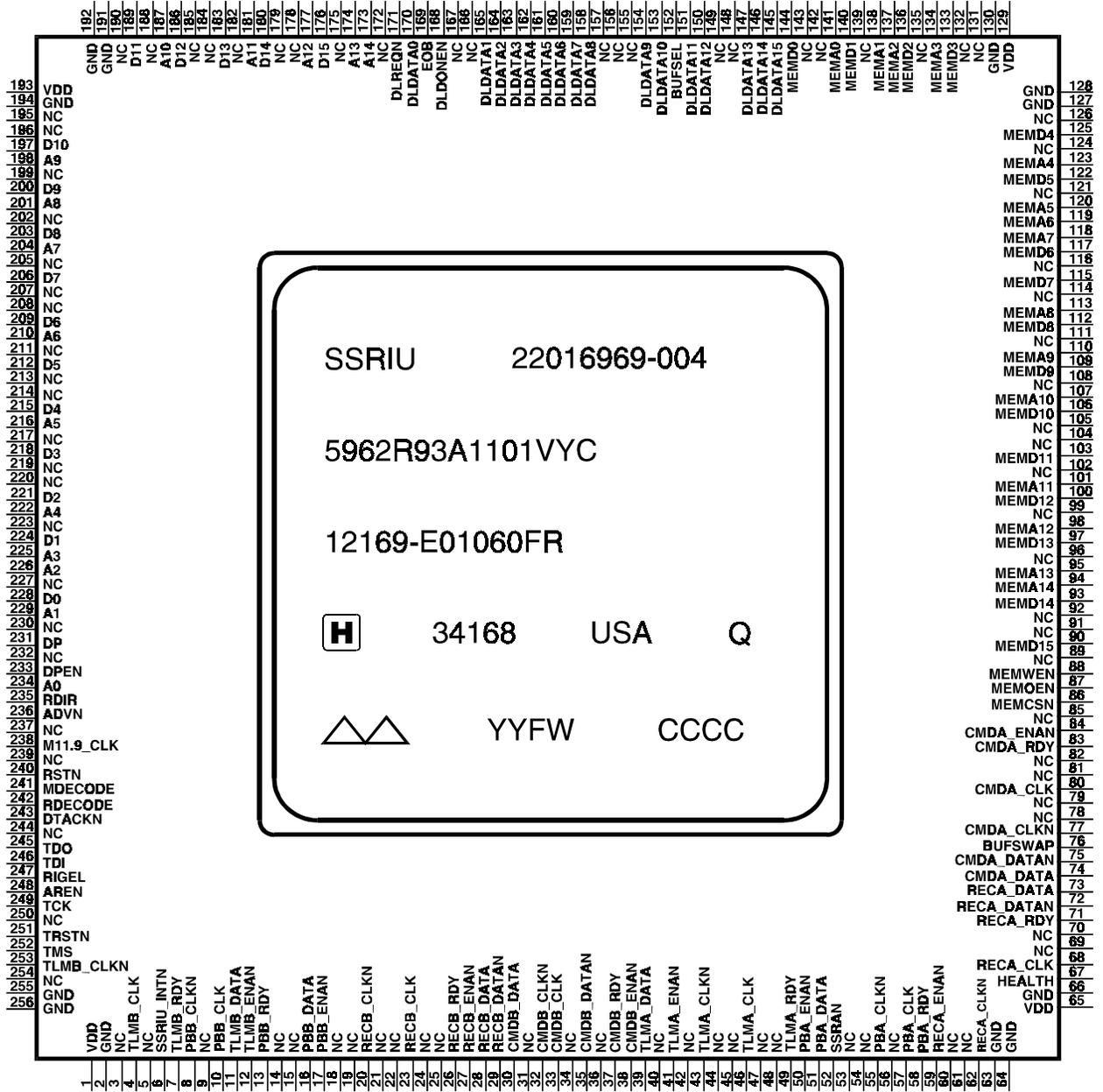


Figure 5-1. SSRIU ASIC Pinout Assignments

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ST 12169	REV. A	TITLE:	ST 12169
		MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	REV. A
SHEET 31		SHEET 31	

5.2 Bonding Diagram

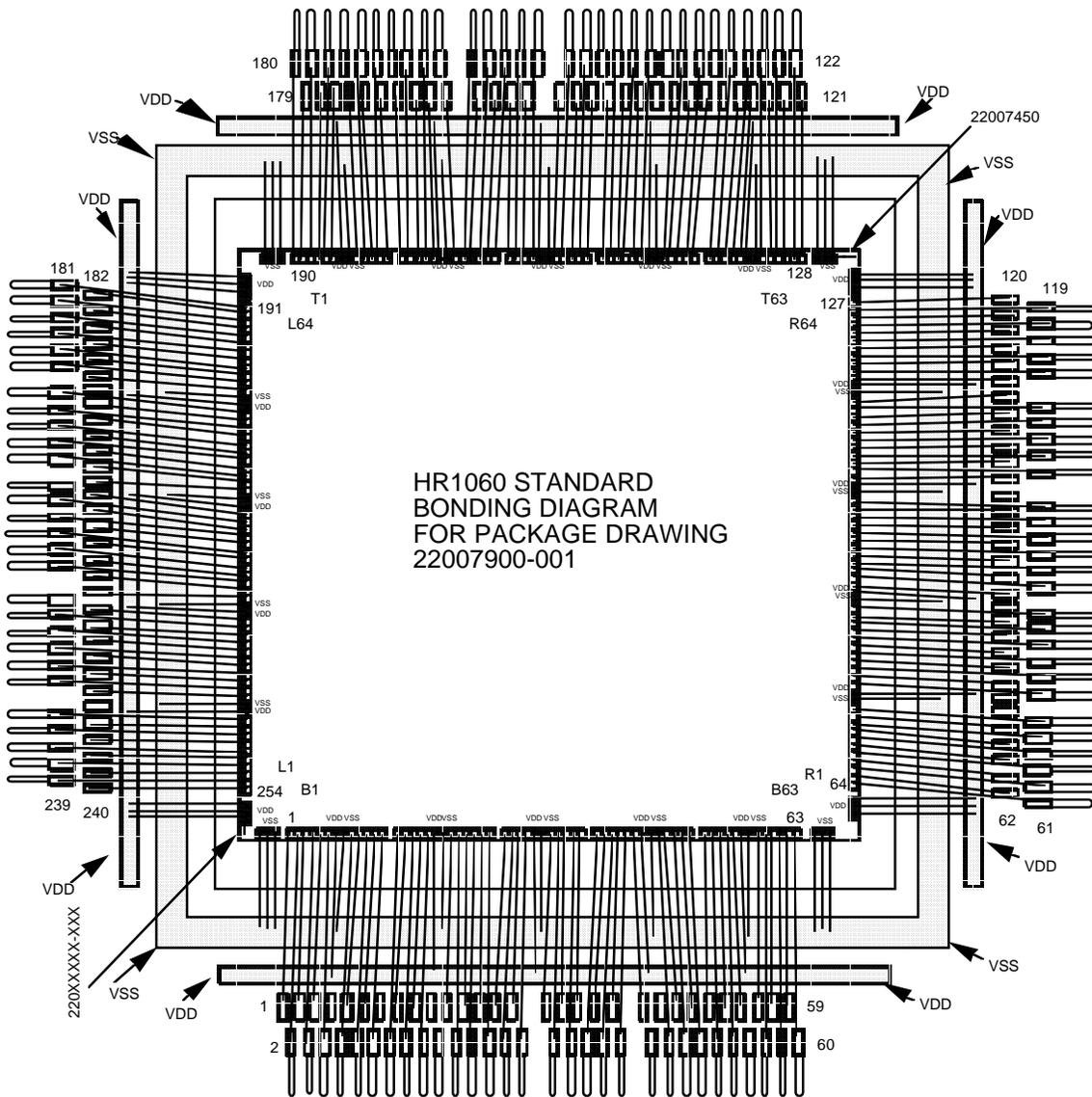
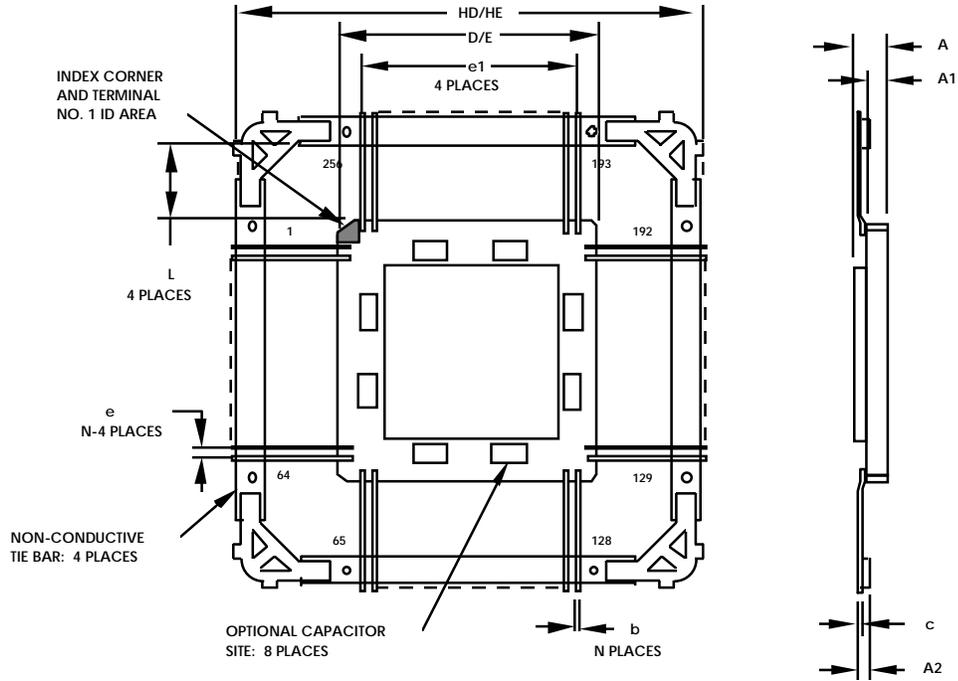


Figure 5-2. Bonding Diagram (256 pin Flatpack)

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 32		SHEET 32	

5.3 Package Outline.

256 Lead Flat Package



PACKAGE DIMENSIONS		
Symbol	Dimensions In Inches	
	min	max
A	0.130	0.160
A1	-	0.130
A2	0.024	0.040
b	0.005	0.009
c	0.004	0.008
D/E	1.445	1.455
e	0.020 BSC	
e1	1.260 BSC	
HD/HE	2.365	2.395
L	0.325	-
N	256	

Figure 5-3. Package Outline (256 pin Flatpack)

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ST 12169	REV. A	TITLE:	ST 12169 REV. A
SHEET 33		MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	SHEET 33

5.4 Marking Diagram

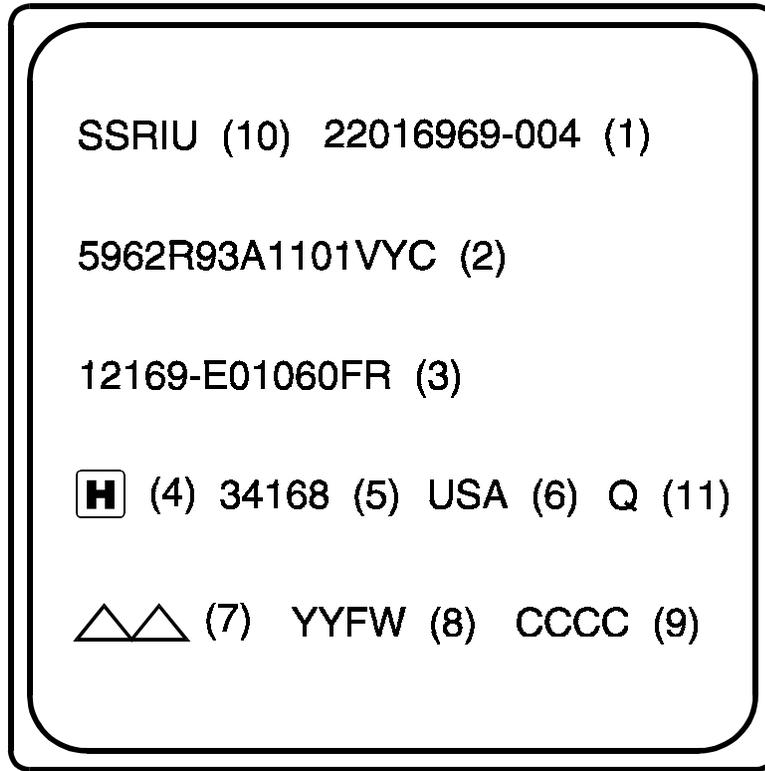


Figure 5-4. Marking Diagram

- (1) Honeywell Part Number
- (2) QML Number (Flight Units only)
- (3) Customer Part Number
- (4) Honeywell Trademark
- (5) Federal Supplier Manufacturing Number
- (6) Country of Origin
- (7) Pin 1 indicator and ESD identifier
- (8) Date Code -Year and Fiscal Week of Lid Seal.
YY = Year
FW = Fiscal Week
- (9) Serialization (Traceability Capability to Die)
- (10) Chip Name (If required)
- (11) QML Mark (Flight Units only)

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ST 12169	REV. A	TITLE: MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, SOLID STATE RECORDER INTERFACE UNIT (SSRIU)	ST 12169 REV. A
SHEET 34			SHEET 34

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